

## **WHAT IS CLAIMED IS:**

1. An integrated circuit architecture comprising  
an array of vertical FET selection transistors formed in a substrate in the form of parallel active webs made of semiconductor material arranged in a lateral direction of the circuit, wherein selection transistor drain terminals are formed by conductive strips buried below the active webs, and  
wherein selection transistor gates are formed by a spacer etched vertically at the side of the active webs;  
an array of memory cells each comprising a storage capacitor, wherein a buried strip makes contact with an electrode of the storage capacitor;  
a wordline for the memory cells of the memory array formed by the vertically etched spacer, wherein each storage capacitor is formed in a deep trench, which in each case delimits on an end side a section of the active web that contains the selection transistor, and which is filled with conductive electrode material;  
a test structure integrated into the integrated circuit architecture, wherein the test structure includes a connection for common connection of the drain terminals of a plurality of vertical selection transistors, as first connecting means, wherein the first connecting means comprises ) diagonally extended deep trenches filled with the conductive electrode material, deposited between two adjacent laterally offset vertical FET transistors, wherein the buried strips present there form drain electrodes of the vertical selection transistors at the intersection of the buried strip form with the diagonally extended deep trench and active web.

2. The integrated circuit architecture of claim 1, wherein the test structure includes a second connecting means for common connection of the source electrodes of the vertical selection transistors, encompassed by the test structure.

3. The integrated circuit architecture of claim 2, wherein the second connecting means comprises bit line contacts and bit lines of the vertical selection transistors.

4. The integrated circuit arrangement of claim 1, wherein the adjacent selection transistors are laterally offset by in each case at least one cell unit, and wherein in each case one deep trench is extended diagonally between in each case two laterally offset vertical selection transistors.

5. The integrated circuit of claim 4, wherein the at least one cell unit comprises a plurality of cell units.

6. The integrated circuit architecture of claim 1, wherein the test structure has a plurality of chains of a multiplicity of vertical selection transistors that are in each case connected to one another, wherein the diagonally extended deep trenches of each chain form a zigzag course between the selection transistors that are connected to one another.

7. The integrated circuit architecture of claim 6, wherein the number of selection transistors of each chain that are connected to one another by the test structure varies significantly between chains.

8. The integrated circuit arrangement of claim 1, wherein two outermost selection transistors of a chain of the test structure are connected by their source terminals to a respectively associated bit line separately by CB contacts.

9. An integrated circuit architecture comprising:  
an memory array including an array of memory cells, wherein each cell comprises a vertical FET selection transistor associated with a trench capacitors, and wherein the selection transistors are formed in active webs such that the drain terminals of the selection transistors are formed by conductive strips buried below the active webs; and  
a test structure integrated into the integrated circuit architecture, wherein the test structure includes a first connection means for common connection of the drain terminals of a plurality of vertical selection transistors,  
wherein the first connection means comprises diagonally extended deep trenches filled with a conductive electrode material, deposited between two adjacent laterally offset vertical FET transistors, and wherein buried strips present there form drain electrodes of the vertical selection transistors at the intersection of the buried strip form with the diagonally extended deep trench and active web.

10. The integrated circuit architecture of claim 9, wherein the test structure includes a second connecting means for common connection of the source electrodes of the vertical selection transistors, encompassed by the test structure.

11. The integrated circuit architecture of claim 10, wherein the second connecting means comprises bit line contacts and bit lines of the vertical selection transistors.

12. The integrated circuit arrangement of claim 9, wherein the adjacent selection transistors are laterally offset by in each case at least one cell unit, and wherein in each case one deep trench is extended diagonally between in each case two laterally offset vertical selection transistors.

13. The integrated circuit of claim 12, wherein the at least one cell unit comprises a plurality of cell units.

14. The integrated circuit architecture of claim 9, wherein the test structure has a plurality of chains of a multiplicity of vertical selection transistors that are in each case connected to one another, wherein the diagonally extended deep trenches of each chain form a zigzag course between the selection transistors that are connected to one another.

15. The integrated circuit architecture of claim 14, wherein the number of selection transistors of each chain that are connected to one another by the test structure varies significantly between chains.

16. An integrated circuit architecture comprising:  
a memory array including vertical FET selection transistors formed in active webs made of semiconductor material; and

a test structure integrated into the integrated circuit architecture, wherein the test structure includes a first connection means for common connection of drain terminals of a plurality of vertical selection transistors,

wherein the first connection means comprises diagonally extended deep trenches filled with a conductive electrode material, deposited between two adjacent laterally offset vertical FET transistors, and wherein buried strips present there form drain electrodes of the vertical selection transistors at the intersection of the buried strip form with the diagonally extended deep trench and active web.

17. The integrated circuit architecture of claim 16, wherein the test structure includes a second connecting means for common connection of the source electrodes of the vertical selection transistors, encompassed by the test structure.

18. The integrated circuit architecture of claim 17, wherein the second connecting means comprises bit line contacts and bit lines of the vertical selection transistors.

19. The integrated circuit arrangement of claim 16, wherein the adjacent selection transistors are laterally offset by in each case at least one cell unit, and wherein in each case one deep trench is extended diagonally between in each case two laterally offset vertical selection transistors.

20. The integrated circuit of claim 18, wherein the at least one cell unit comprises a plurality of cell units.